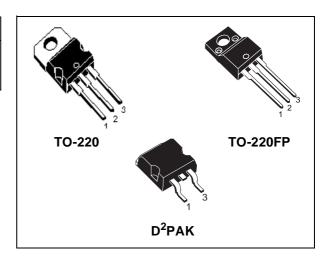


STP11NK40Z - STP11NK40ZFP STB11NK40Z

N-CHANNEL 400V - 0.49Ω - 9A TO-220/TO-220FP/D²PAK Zener-Protected SuperMESH™Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	Pw
STP11NK40Z	400 V	< 0.55 Ω	9 A	110 W
STP11NK40ZFP	400 V	< 0.55 Ω	9 A	30 W
STB11NK40Z	400 V	< 0.55 Ω	9 A	110 W

- TYPICAL R_{DS}(on) = 0.49 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

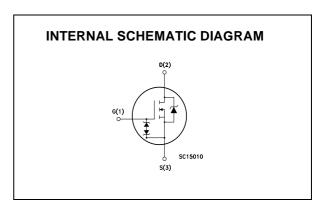


DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP11NK40Z	P11NK40Z	TO-220	TUBE
STP11NK40ZFP	P11NK40ZFP	TO-220FP	TUBE
STB11NK40ZT4	B11NK40Z	D ² PAK	TAPE & REEL

April 2003 1/12

STP11NK40Z - STP11NK40ZFP - STB11NK40Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Valu	е	Unit
		STP11NK40Z STB11NK40Z	STP11NK40ZFP	
V_{DS}	Drain-source Voltage (V _{GS} = 0)	400		V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	400		V
V_{GS}	Gate- source Voltage	± 30)	V
I _D	Drain Current (continuous) at T _C = 25°C	9	9(*)	Α
I _D	Drain Current (continuous) at T _C = 100°C	5.67	5.67(*)	Α
I _{DM} (•)	Drain Current (pulsed)	36	36(*)	А
P _{TOT}	Total Dissipation at T _C = 25°C	110	30	W
	Derating Factor	0.88	0.24	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3500)	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
Viso	Insulation Withstand Voltage (DC)	2500		V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

^(●) Pulse width limited by safe operating area

THERMAL DATA

		TO-220 D ² PAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1.14	4.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.	5	°C/W
TI	Maximum Lead Temperature For Soldering Purpose	300)	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	9	А
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	190	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

⁽¹⁾ I_{SD} \leq 9A, di/dt \leq 200A/ μ s, V_{DD} \leq V(BR)DSS, T $_{j}$ \leq T_{JMAX}.

^(*) Limited only by maximum temperature allowed

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	400			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_{C} = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 4.5 A		0.49	0.55	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 4.5 A		5.8		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		930 140 30		pF pF pF
Coss eq. (3)	Equivalent Output Capacitance	V _{GS} = 0 V, V _{DS} = 0 V to 400 V		78		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V_{DD} = 200 V, I_D = 4.5 A R_G = 4.7 Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		20 20		ns ns
$egin{array}{c} Q_g \ Q_{gs} \ Q_{gd} \end{array}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 320 \text{ V}, I_{D} = 9 \text{ A}, V_{GS} = 10 \text{ V}$		32 6 18.5	45	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V_{DD} =200 V, I_{D} = 4.5 A R _G = 4.7 Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		40 18		ns ns
$\begin{array}{c} t_{r(\text{Voff})} \\ t_{f} \\ t_{c} \end{array}$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 320 \text{ V, } I_D = 9 \text{ A,}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (Inductive Load see, Figure 5)		15 17 30		ns ns ns

SOURCE DRAIN DIODE

Symbol	pol Parameter Test Conditions M		Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				9 36	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 9 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 9 A, di/dt = 100 A/ μ s V_{DD} =45 V, T_j = 150°C (see test circuit, Figure 5)		225 1.6 14		ns μC A

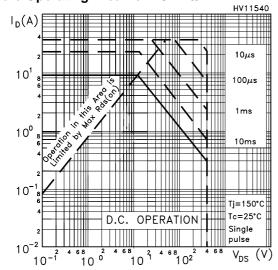
Note: 1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.

3/12

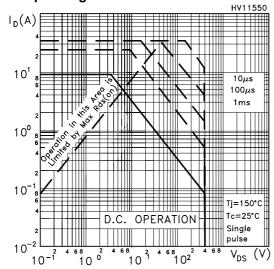
<u>57</u>

r uise uuration = 300 µs, duty cycle 1.5 %.
 Pulse width limited by safe operating area.
 C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSs}.

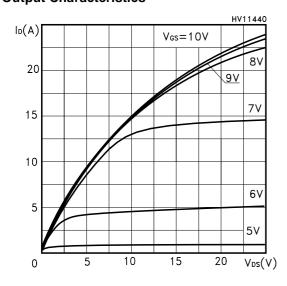
Safe Operating Area For TO-220/D2PAK



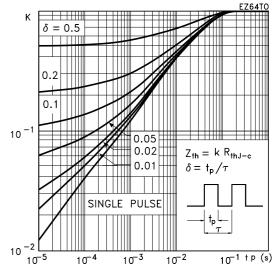
Safe Operating Area For TO-220FP



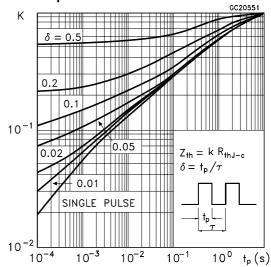
Output Characteristics



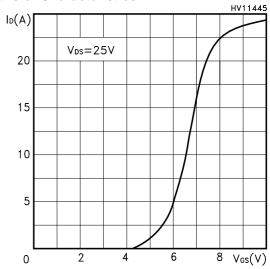
Thermal Impedance For TO-220/D2PAK



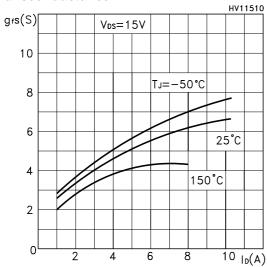
Thermal Impedance For TO-220FP



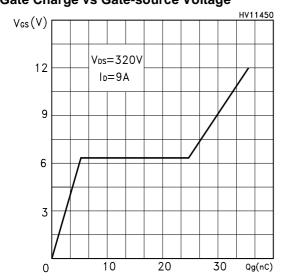
Transfer Characteristics



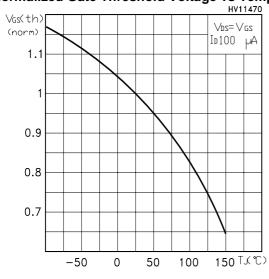
Transconductance



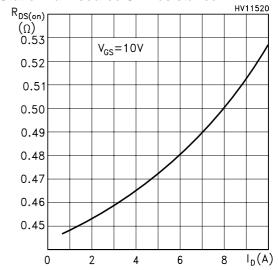
Gate Charge vs Gate-source Voltage



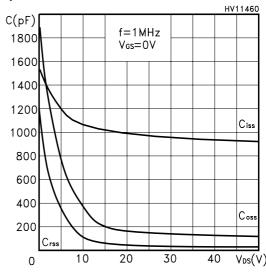
Normalized Gate Threshold Voltage vs Temp.



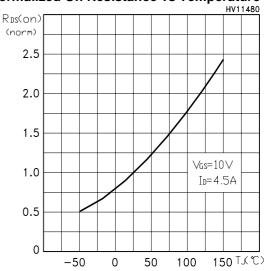
Static Drain-source On Resistance



Capacitance Variations

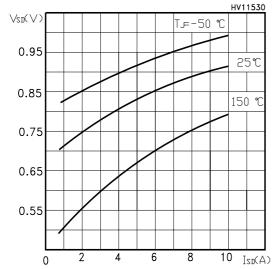


Normalized On Resistance vs Temperature

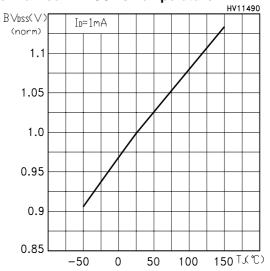


STP11NK40Z - STP11NK40ZFP - STB11NK40Z

Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature HV11500

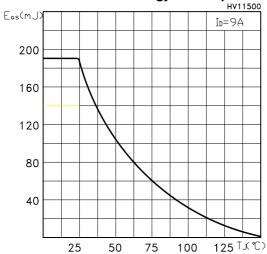


Fig. 1: Unclamped Inductive Load Test Circuit

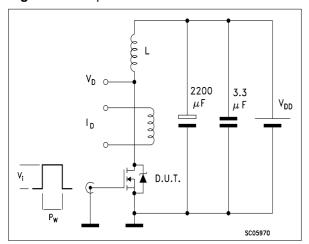


Fig. 3: Switching Times Test Circuit For Resistive Load

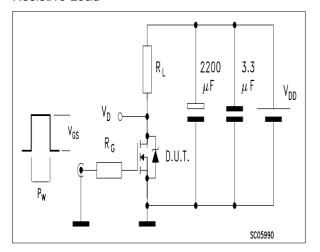


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

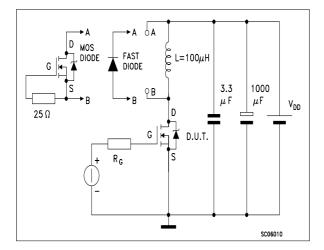


Fig. 2: Unclamped Inductive Waveform

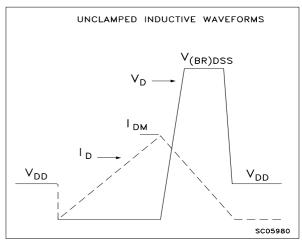
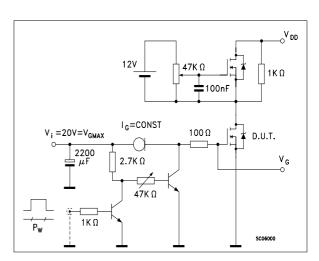
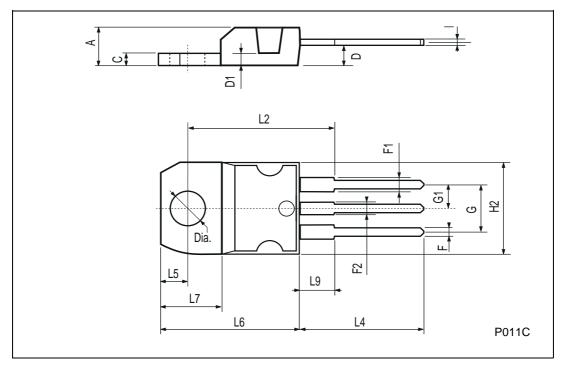


Fig. 4: Gate Charge test Circuit



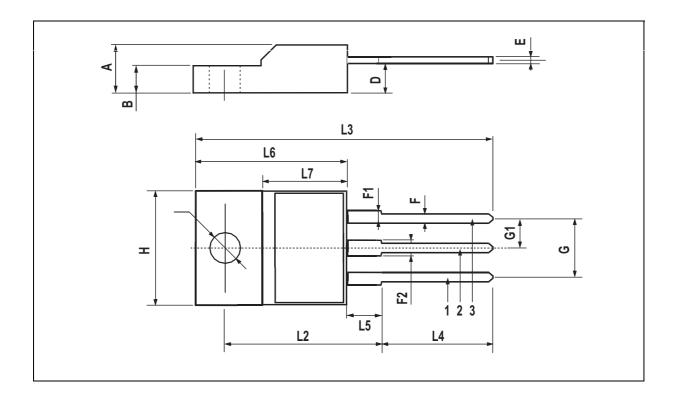
TO-220 MECHANICAL DATA

DIM.		mm			inch	
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α	4.40		4.60	0.173		0.181
С	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
Е	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



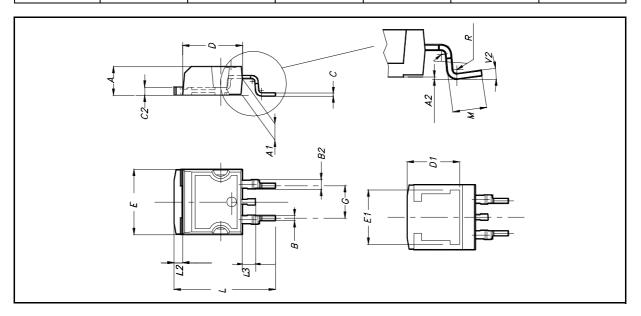
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А	4.4		4.6	0.173		0.181
В	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
Е	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
Н	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
В	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
С	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
Е	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
М	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



D²PAK FOOTPRINT

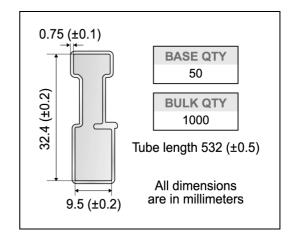
- 9.75 -

→3.50 ←

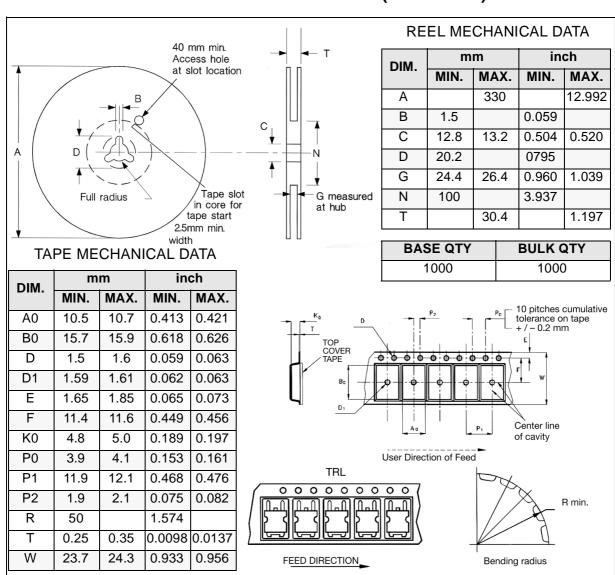
All dimensions

are in millimeters

TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States. © http://www.st.com